Complex Digital Logic and FPGA Capabilities

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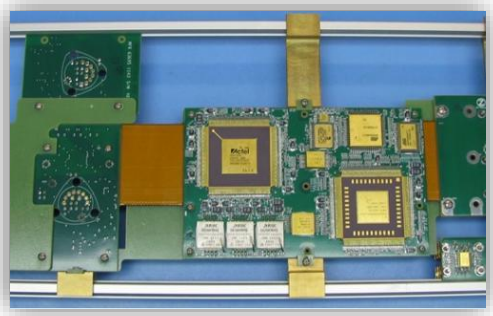
Performance - For the NASA GSFC MMS mission ZIN provided a triple mode redundant digital logic implementation with the following functions: 16-bit ADC interfaces, FIR filter for acceleration memory mapped registers, CPU reset for unrecoverable errors, software directed board-level reset, power rail enables and EEPROM controls. The design was validated to the GSFC process including conducting a Worst Case Circuit Analysis (WCA). The WCA included end of life analysis.

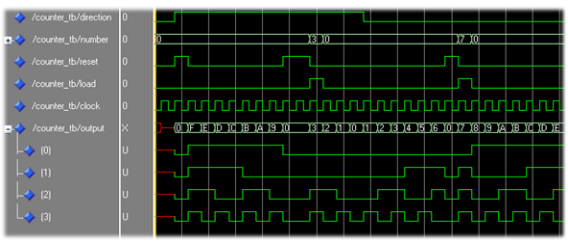
TOOLS:

- FPGA Breadboard (Actel PROASIC 3E Development Kit)
- RTAX1000-CQ352M (Flight) & AX1000-FG896 (ETU)
- Tools: Actel's Libero IDE (v9.0.3.7)
- Synthesis: Synplicity's Synplify Pro (D-2009.12A)
- Simulation: Mentor Graphics' ModelSIM ACTEL 6.5d (v2009.11)
- Place&Route: Actel Designer Software(v9.0.3.7)
- Static Timing: Actel's SmartTime (v9.0 SP3A)
- Programming: BP Microsystems' SculptW (v5.10.0 w/ Silicon Sculptor II)
- Electronics Control Loop Design
- MATLAB and Simulink

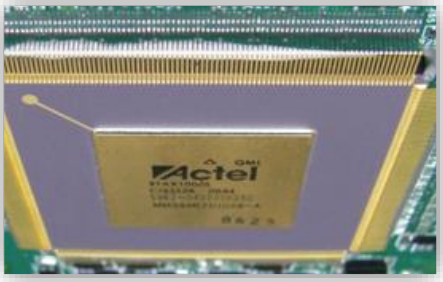


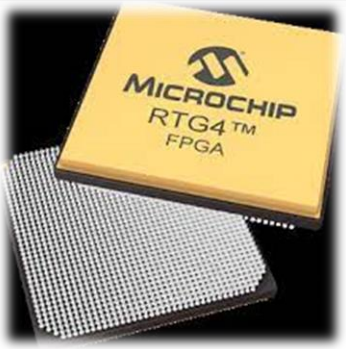
ZIN has digital logic design experience including work in FPGA implementation and ASIC development. ZIN has provided logic design, simulation, and implementation of FPGA designs, in Very High Density Logic (VHDL) and Verilog, including fault tolerant designs with Finite Impulse Response (FIR) filters and interface controllers that used Triple Modular Redundancy (TMR) with error correction for non-hardened static random-access memory (SRAM) blocks. ZIN is compliant to the GSFC FPGA design and validation process.

ZIN develops circuits, mixed signal boards, and single board computers for embedded systems. This involves the design, analysis, and fabrication of digital and mixed signal based solution for space-rated, radiation tolerant systems. ZIN has experience implementing Fault-Tolerant 32-bit LEON3 processor ASIC (UT-699) and the radiation hardened FPGA (RTAX-S) on a single custom rigid-flex Printed Wiring Assembly (PWA). Designed to IPC 6013 Class 3 standards.



- **ZIN has extensive digital logic design experience including proficiency in FPG implementation and ASIC development.**
- **ZIN has provided logic design, simulation, and implementation of FPGA designs, in VHDL and Verilog, including fault tolerant designs for Mission Critical applications.**
- **ZIN is compliant to the GSFC FPGA design and validation process and NASA-HDBK-4008.**





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